Amendments to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

1. (currently amended) A semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a fin formed on the insulating layer, the fin having a plurality of side surfaces, a top surface and a bottom surface;

an oxide layer formed over the top surface of the fin;

a nitride layer formed over the oxide layer; and

a gate formed on the insulating layer, the gate surrounding the plurality of side surfaces, the top surface and the bottom surface of the fin at a channel region of the semiconductor device.

2. (currently amended) The semiconductor device of claim 1, wherein the gate comprises a first gate electrode disposed on a first side of the fin and a second gate electrode disposed on a second side of the fin opposite the first side.

3. (currently amended) The semiconductor device of claim 2, wherein ~~a portion of~~ the gate comprises a third gate electrode surrounding the bottom surface of the fin ~~comprises a third gate~~.

4. (currently amended) The semiconductor device of claim 3, wherein ~~a portion of~~ the gate comprises a fourth gate electrode surrounding the top surface of the fin ~~comprises a fourth gate~~.

5. (original) The semiconductor device of claim 1, further comprising:

a first dielectric layer formed around the plurality of side surfaces and the bottom surface of the fin.

6. (canceled)

7. (currently amended) The semiconductor device of claim [[6]] 1, wherein ~~the at least one dielectric layer comprises:~~

~~an~~ the oxide layer ~~formed over the top surface of the fin~~ has a thickness ranging from about 20 Å to about 400 Å, and

[[a]] the nitride layer ~~formed over the oxide layer~~ has a thickness ranging from about 100 Å to about 800 Å.

8. (currently amended) The semiconductor device of claim [[7]] 5, wherein the first dielectric layer has a thickness ranging from about 8 Å to about 50 Å~~, the oxide layer has a thickness ranging from about 20 Å to about 400 Å and the nitride layer has a thickness ranging from about 100 Å to about 800 Å~~.

9. (currently amended) The semiconductor device of claim 1, further comprising:

a source region and a drain region formed above the insulating layer and adjacent a respective first and second end of the fin, wherein the insulating later comprises a buried oxide layer and the fin comprises at least one of silicon ~~and~~ or germanium.

10-14. (canceled)

15. (original) A semiconductor device, comprising:

a substrate;

an insulating layer disposed on the substrate;

a conductive fin formed on the insulating layer, the conductive fin having a first end, a second end and a middle portion located between the first and second ends, wherein the first and second ends are disposed on the insulating layer and the middle portion is separated from the insulating layer;

at least one dielectric layer formed over a top surface of the conductive fin;

a gate dielectric layer formed on side surfaces and a bottom surface of the conductive fin; and

a gate formed on the insulating layer, the gate surrounding the gate dielectric layer formed on the side surfaces and bottom surface at the middle portion of the conductive fin and covering the at least one dielectric layer formed over the top surface at the middle portion of the conductive fin.

16. (original) The semiconductor device of claim 15, wherein the gate comprises a first gate electrode disposed on a first side of the conductive fin and a second gate electrode disposed on an opposite side of the conductive fin.

17. (original) The semiconductor device of claim 16, wherein the gate further comprises a third gate electrode disposed on a bottom side of the conductive fin.

18. (original) The semiconductor device of claim 17, wherein the gate further comprises a fourth gate electrode disposed on a top side of the conductive fin.

19. (original) The semiconductor device of claim 15, wherein the at least one dielectric layer comprises:

an oxide layer having a thickness ranging from about 20 Å to about 400 Å, and

a nitride layer having a thickness ranging from about 100 Å to about 800 Å.

20. (original) The semiconductor device of claim 15, further comprising:

a source region and a drain region formed above the insulating layer and adjacent a respective first and second end of the fin, wherein the gate dielectric layer has a thickness ranging from about 8 Å to about 50 Å.

21. (new) A semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a fin formed on the insulating layer, the fin having a plurality of side surfaces, a top surface and a bottom surface;

a dielectric layer formed around the plurality of side surfaces and the bottom surface of the fin, the dielectric layer having a thickness ranging from about 20 Å to about 50 Å; and

a gate formed on the insulating layer, the gate surrounding the plurality of side surfaces, the top surface and the bottom surface of the fin at a channel region of the semiconductor device.

22. (new) The semiconductor device of claim 21, further comprising:

an oxide layer formed over the top surface of the fin; and

a nitride layer formed over the oxide layer.

23. (new) The semiconductor device of claim 21, further comprising:

a source region and a drain region formed above the insulating layer and adjacent a respective first and second end of the fin, wherein the insulating later comprises a buried oxide layer and the fin comprises at least one of silicon or germanium.

24. (new) The semiconductor device of claim 21, wherein the gate comprises a first gate electrode disposed on a first side of the fin and a second gate electrode disposed on a second side of the fin opposite the first side.